What is claimed is:

1. A method for characterizing a timing delay curve of a circuit component, said timing delay curve having a first region and a second region, comprising:

determining a first delay equation representing said first region of the delay curve;

determining a second delay equation representing said second region of the delay curve; and

determining a corner capacitance of said circuit component, said corner capacitance representing a transition point from said first region to said second region.

2. The method of claim 1 wherein said determining a first delay equation further comprises:

creating a model of said circuit component, said model having a variable resistance, said variable resistance changing substantially linearly between a maximum resistance and a minimum resistance; and

deriving an equation for the delay of said model for $0 < t < \tau$, where t represents time and τ represents an input signal edge time.

3. The method of claim 2 wherein said deriving an equation step further comprises:

determining an equation for the gradient of a linear change between said maximum resistance and said minimum resistance of said variable resistance.

4. The method of claim 1 wherein said determining said second delay equation further comprises:

creating a model of said circuit component, said model having a variable resistance, said variable resistance changing substantially linearly between a maximum resistance and a minimum resistance; and

deriving an equation for the delay of said model for $t \lesssim \tau$, where t represents time and τ represents an input signal edge time.

5. The method of claim 1 wherein said determining the corner capacitance step further comprises:

setting said first delay equation equal to said second delay equation; and

solving said first delay equation and said second delay equation for the capacitance.

6. The method of claim 1 wherein said determining a first delay equation further comprises:

determining a delay equation for a curvilinear region of the delay curve.

7. The method of claim 1 wherein said determining a second delay equation further comprises:

determining a delay equation for a linear region of the delay curve.

8 The method of claim 1 wherein said determining a first delay equation further comprises:

setting the delay, d, of said circuit component equal to $\frac{\tau}{1-f}\left[1-2^{-(1-f)RC/\tau}\right]$, where R represents the variable resistance of said component, C represents a capacitance of said component, τ represents an input signal edge time, and f represents a constant fraction between zero and one.

9. The method of claim 1 wherein said determining a second delay equation further comprises:

setting the delay, d, of said circuit component equal to $fRC\ln 2$, where R represents the variable resistance of said component, C represents the capacitance of said component, and f represents a constant fraction between zero and one.